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STRUCTURES AND METHODS FOR MAN-UFACTURING STRAINED P-TYPE MOSFET WITH GRADED EMBEDDED SILICON-GERMANIUM SOURCE-DRAIN EXTENSION

Abstract

P-type MOSFETs (PMOSFETs) are formed by encapsulating the gate with an insulator and depositing a germanium containing layer outside the sidewalls, then diffusing the germanium into the sili-con-on-insulator layer or bulk silicon by annealing or by oxidiz-ing to form graded embedded silicon-germanium source-drain and/or Extension (geSiGe-SDE). For SOI devices, the geSiGe-SDE is allowed to reach the buried insulator to maximize the stress in the channel of SOI devices, which is beneficial for ultra-thin SOI de-vices. Graded germanium profiles provide a method to optimize stress in order to enhance device performance. The geSiGe-SDE creates a compressive stress in the horizontal direction (parallel to the gate dielectric surface) and tensile stress in the vertical direc-tion (normal to the gate dielectric surface) in the channel of the PMOSFET, therebyforming a structure that enhances PMOSFET

performance.